Claims:

1. A method of making an SOI device having a gate with one or more additional gate regions, comprising the steps of:

implanting oxygen or halogen ions in a substrate of an SOI device;

forming a gate oxide on the substrate, with the gate oxide being thicker by having the oxygen or halogen ions providing gate oxide regions in the substrate; and

constructing the one or more additional gate regions to cover the gate oxide regions under the one or more additional gate regions.

2. The method as recited in claim 1, further comprising the step of:

implanting ions in the substrate before implanting the oxygen or fluorine ions.

3. The method as recited in claim 1, further comprising the steps of:

implanting ion implants in the substrate before subsequently implanting the oxygen or fluorine ions; and

covering the ion implants in the substrate with the one or more additional drain regions during construction of a source and a drain of the SOI device.

4. The method as recited in claim 1, further comprising the steps of:

constructing a gate oxide layer covering the ions, followed by;

constructing the one or more additional gate regions on the gate oxide layer, and removing the gate oxide layer except where the gate oxide layer is under the one or more additional gate regions.

5. The method as recited in claim 1, further comprising the steps of:

constructing a gate oxide layer covering the ions, followed by;

constructing an SOI device gate and the one or more additional gate regions on the gate oxide layer; and thereafter removing the gate oxide layer except where the gate oxide layer is under the gate and under the one or more additional gate regions.

6. The method as recited in claim 1, further comprising the steps of:

constructing a gate oxide layer covering the ions, followed by;

constructing a gate electrode layer covering the gate oxide layer;

selectively removing the gate electrode layer to form an SOI device gate and the one or more additional gate regions; and

thereafter removing the gate oxide layer except where the gate oxide layer is under the gate and under the one or more additional gate regions.

7. The method as recited in claim 1, further comprising the steps of:

constructing a gate oxide layer covering the ions, followed by;

constructing a gate electrode layer covering the gate oxide layer; and

selectively removing the gate electrode layer to form an SOI device gate and the one or more additional gate regions, while removing the gate oxide layer except where the gate oxide layer is under the gate and under the one or more additional gate regions.

8. The method as recited in claim 1, further comprising the steps of:

constructing a thin gate oxide layer having a thicker gate oxide covering the ions; followed by;

constructing an SOI device gate on the thin gate oxide layer, while constructing the one or more additional gate regions on the thicker gate oxide; and removing the thin gate oxide layer except where the thin gate oxide layer is under the gate.

9. The method as recited in claim 8, further comprising the steps of: constructing the thicker gate oxide by selective epitaxy.

10. The method as recited in claim 1, further comprising the step of: constructing an STI enclosure for the ions.

11. An SOI device having a gate, comprising:

oxygen or halogen ions providing implants in a substrate of an SOI device; and

one or more additional gate regions covering all implants under the one or more additional gate regions, the ions forming thicker gate oxide regions, and reducing substrate resistance under each of the gate regions.

12. The SOI device as recited in claim 11, further comprising:

implanted ions in the substrate, the one or more additional gate regions covering the implanted ions.

13. The SOI device as recited in claim 11, further comprising:

a gate oxide covering the ions and being under the one or more additional gate regions.

14. The SOI device as recited in claim 11, further comprising:

a gate of the SOI device;

a gate oxide under the gate and under the one or more additional gate regions; and

the gate oxide covering the ions.

15. The SOI device as recited in claim 11, further comprising:

a gate electrode layer forming an SOI device gate and the one or more additional gate regions; and

a gate oxide layer under the gate and under the one or more additional gate regions.

16. The SOI device as recited in claim 11, further comprising:

an SOI device gate and the one or more additional gate regions being formed from a gate electrode layer; and

a gate oxide layer wherein the gate oxide layer is under the gate and under the one or more additional gate regions.

17. The SOI device as recited in claim 11, further comprising:
a thin gate oxide layer having a thicker gate oxide covering the ions;
an SOI device gate on the thin gate oxide layer; and
the one or more additional gate regions being on the thicker gate oxide.

18. The SOI device as recited in claim 11, further comprising:
the thicker gate oxide being a selective epitaxy growth.

19. The SOI device as recited in claim 11, further comprising:
the substrate having an STI enclosure for the ions.

20. An SOI device in a substrate on a semiconductor wafer, comprising:
a semiconductor layer as part of the substrate;
an additional gate electrode on the substrate; and
oxygen ions in the substrate forming implants in a gate oxide region under the additional gate electrode.

21. The SOI device of claim 20, further comprising:
doped ion implants under the gate electrode, the doped ion implants forming a source and drain in the substrate.

22. The SOI device of claim 20, further comprising:
a buried oxide layer covering the semiconductor wafer; and
the semiconductor layer being on the buried oxide layer.

23. The SOI device of claim 20 wherein, the semiconductor layer is a P-substrate, and the doped ion implants are N+ doped ions.

24. The SOI device of claim 20 wherein, the semiconductor layer is an N-substrate, and the doped ion implants are P+ doped ions.

25. The SOI device of claim 20, further comprising:
at least one additional gate region on the gate electrode; and
the oxygen ions forming a thick gate oxide region under said additional gate region.

26. The SOI device of claim 20, further comprising:
additional gate regions on the gate electrode forming an H-gate; and
the oxygen ions forming shallow trench isolation regions.

27. An SOI device in a substrate on a semiconductor wafer, comprising:
a semiconductor layer as part of the substrate;
a gate electrode on the substrate; and
halogen ions in the substrate forming implants in a gate oxide region under the gate electrode.

28. The SOI device of claim 27, further comprising:
doped ion implants under the gate electrode, the doped ion implants forming a source and drain in the substrate;

29. The SOI device of claim 27, further comprising:
a buried oxide layer covering the semiconductor wafer; and
the semiconductor layer being on the buried oxide layer.

30. The SOI device of claim 27 wherein, the semiconductor layer is a P-substrate, and the doped ion implants are N+ doped ions.

31. The SOI device of claim 27 wherein, the semiconductor layer is an N-substrate, and the doped ion implants are P+ doped ions.

32. The SOI device of claim 27, further comprising:
at least one additional gate region on the gate electrode; and
the halogen ions forming a thick gate oxide region under said additional gate region.

33. The SOI device of claim 27, further comprising:
additional gate regions on the gate electrode forming an H-gate; and
the halogen ions forming shallow trench isolation regions.

34. The SOI device of claim 27 wherein, the halogen ions are fluorine ions.